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of

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for

GATE STACK STRUCTURE

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This is a divisional application of US Patent Application Serial No. 08/846,671, filed on April 20, 1997, titled "UNDOPED SILICON DIOXIDE AS ETCH STOP FOR SELECTIVE ETCH OF DOPED SILICON DIOXIDE", which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. The Field of the Invention

The present invention involves an etching process that utilizes an undoped silicon dioxide layer as an etch stop during a selective etch of a doped silicon dioxide layer that is situated on a semiconductor substrate. More particularly, the present invention relates to a process for selectively utilizing a fluorinated chemistry in a plasma etch system for etching a doped silicon dioxide layer situated upon an undoped silicon dioxide layer that acts as an etch stop.

2. The Relevant Technology

Modern integrated circuits are manufactured by an elaborate process in which a large number of electronic semiconductor devices are integrally formed on a semiconductor substrate. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including but not limited to bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term substrate refers to any supporting structure including but not limited to the semiconductive substrates described above.

Conventional semiconductor devices which are formed on a semiconductor substrate include capacitors, resistors, transistors, diodes, and the like. In advance manufacturing of integrated circuits, hundreds of thousands of these semiconductor devices are formed on a single semiconductor substrate. In order to compactly form the semiconductor devices, the

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semiconductor devices are formed on varying levels of the semiconductor substrate. This requires forming a semiconductor substrate with a topographical design.

The semiconductor industry is attempting to increase the speed at which integrated circuits operate, to increase the density of devices on the integrated circuits, and to reduce the price of the integrated circuits. To accomplish this task, the semiconductor devices used to form the integrated circuits are continually being increased in number and decreased in dimension in a process known as miniaturization.

One component of the integrated circuit that is becoming highly miniaturized is the active region. An active region is a doped area in a semiconductor substrate that is used together with other active regions to form a diode or a transistor. The miniaturization of the active region complicates the formation of the interconnect structure in that, in order to maintain sufficient electrical communication, the interconnect structure must be formed in exact alignment with the active region. Also, the area of the interconnect structure interfacing with the active region must be maximized. Thus, less area is provided as tolerance for misalignment of the interconnect structure.

The increasing demands placed upon manufacturing requirements for the interconnect structure have not been adequately met by the existing conventional technology. For example, it is difficult at greater miniaturization levels to exactly align the contact hole with the active region when patterning and etching the contact hole. As a result, topographical structures near the bottom of the contact hole upon the active region can be penetrated and damaged during etching of the contact hole. The damage reduces the performance of the active region and alters the geometry thereof, causing a loss of function of the semiconductor device being formed and possibly a defect condition in the entire integrated circuit. To remedy these problems, the prior art uses an etch stop to prevent over etching.

In a conventional self-aligned etch process for a contact hole, a silicon nitride layer or cap is usually used on top of a gate stack as an etch stop layer during the self-aligned

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contact etch process. One of the problems in the prior art with forming a silicon nitride cap was the simultaneous formation of a silicon nitride layer on the back side of the semiconductor wafer. The particular problems depend on the process flow. For instance, where a low pressure chemical vapor deposition is used to deposit silicon nitride, both sides of the semiconductor wafer would receive deposits of silicon nitride. The presence of the silicon nitride on the back side of the semiconductor wafer causes stress which deforms the shape of the semiconductor wafer, and can also potentially cause deformation of the crystal structure as well as cause defects in the circuit. Additionally, silicon nitride deposition is inherently a dirty operation having particulate matter in abundance which tends to reduce yield. When a low pressure chemical vapor deposition process is utilized, the silicon nitride layering on the back side of the semiconductor wafer must be removed later in the process flow.

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SUMMARY OF THE INVENTION

The present invention relates to a process for selectively plasma etching a semiconductor substrate to form a designated topographical structure thereon utilizing an undoped silicon dioxide layer as an etch stop. In one embodiment, a substantially undoped silicon dioxide layer is formed upon a layer of semiconductor material. A doped silicon dioxide layer is then formed upon the undoped silicon dioxide layer. The doped silicon dioxide layer is etched to create a topographical structure. The etch has a material removal rate that is at least 10 times higher for doped silicon dioxide than for the undoped silicon dioxide or the layer of semiconductor material.

One application of the inventive process includes a multilayer structure situated on a semiconductor substrate that comprises layers of a semiconductor material, a thin silicon dioxide layer, a layer of conductor material, and a refractory metal silicide layer. By way of example, the multilayer structure situated on a semiconductor substrate may consist of a gate oxide situated on a silicon substrate, a layer of polysilicon, and a refractory metal silicide layer on the layer of polysilicon. A substantially undoped silicon dioxide layer is then formed over the multilayer structure.

The multilayer structure is then patterned to form the designated topography. Doped silicon dioxide is then formed on the semiconductor substrate as a passivation layer. A photoresist layer is utilized to expose selected portions of the doped silicon dioxide layer that are intended to be etched. One example of a topographical structure created utilizing this process are gate stacks. The doped silicon dioxide is then selectively and anisotropically etched with a carbon fluorine etch recipe so as to self-align contact holes down to the semiconductor substrate between the gate stacks.

Each gate stack has a cap composed of substantially undoped silicon dioxide. A layer of silicon nitride or undoped silicon dioxide is deposited over the gate stacks and the semiconductor substrate therebetween. A spacer etch is performed to create silicon nitride

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or undoped silicon dioxide spacers on the side of each gate stack. The silicon nitride or undoped silicon dioxide spacers are generally perpendicular to the base silicon layer.

The present invention contemplates a plasma etching process for anisotropic etching a doped silicon dioxide layer situated on an undoped silicon dioxide layer that acts as an etch stop. One application of the present invention is the formation of gate stacks having spacers composed of substantially undoped silicon dioxide. The undoped silicon dioxide spacers act as an etch stop. Novel gate structures are also contemplated that use a substantially undoped silicon dioxide etch stop layer for a carbon fluorine etch of a doped silicon dioxide layer, where the substantially undoped silicon dioxide etch stop layer resists etching by a carbon fluorine etch.

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BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which the above-recited and other advantages and objects of the invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are therefore not to be considered limiting of its scope, the invention will be described with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 is a partial cross-sectional elevation view of one embodiment of a multilayer structure prior to an etch, the multi-layer structure including a base silicon layer and a layer of undoped silicon dioxide, where the multi-layer structure has a layer of photoresist, and wherein a first selected pattern is defined in phantom.

Figure 2 is a partial cross-sectional elevation view of the structure seen in Figure 1, wherein the layer of undoped silicon dioxide has been etched so as to form a recess terminating upon the base silicon layer, a layer of doped silicon dioxide has been deposited thereover, where a layer of photoresist is formed over the layer of doped silicon dioxide, and wherein a second selected pattern is defined in phantom which is intended to represent an etch through the layer of doped silicon dioxide to expose a contact on the base silicon layer that is self-aligned between the layer of undoped silicon dioxide, wherein the self-alignment of the etch is due to the selectivity of the etch to undoped silicon dioxide.

Figure 3 is a partial cross-sectional elevation view of one embodiment of a multilayer structure prior to an etch, the multilayer structure including a base silicon layer and having thereon layers of gate oxide, polysilicon, tungsten silicide, and undoped silicon dioxide, where the multi-layer structure has a layer of photoresist, and wherein a first selected pattern is defined in phantom.

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Figure 4 is a partial cross-sectional elevation view of the structure seen in Figure 3, wherein gate stacks are formed upon the base silicon layer, each gate stack having a spacer on a sidewall thereof and a cap on the top thereof, the gate stacks having deposited thereover a layer of doped silicon dioxide, and a layer of photoresist is deposited upon the layer of doped silicon dioxide, wherein a second selected pattern is defined in phantom which is intended to represent a fluorinated chemical etch through the layer of doped silicon dioxide to expose a contact on the base silicon layer that is self-aligned between the gate stacks, wherein the self-alignment of the etch is due to the selectivity of the etch to the materials of the spacers and the cap of the gate stacks.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The inventive process herein is directed towards selectively utilizing a plasma etch system on doped silicon dioxide (SiO_2) layer with a substantially undoped silicon dioxide layer as an etch stop. One application of the inventive process is to form a self-aligned contact. The present invention also discloses an inventive multilayer gate structure.

As illustrated in Figure 1, one embodiment of a multilayer structure 10 is created that comprises a base silicon layer 12. Overlying silicon base layer 12 is a substantially undoped silicon dioxide layer 22. Undoped silicon dioxide layer 22 can be any type of undoped oxide and be formed by a thermal process, by a plasma enhanced deposition process, or by a conventional TEOS precursor deposition that is preferably rich in carbon or hydrogen, or by a precursor of gaseous silane (SiH_4) with oxygen. In the latter process, the gaseous silane flow will result in undoped silicon dioxide layer 22.

The next layer in the embodiment of multilayer structure 10 illustrated in Figure 1 comprises a photoresist layer 24 that is processed to expose a first selected pattern 15, shown in phantom, such that silicon dioxide layer 22 will be used to create a topography in multilayer structure 10. Multilayer structure 10 is then anisotropically etched as shown by first selected pattern 15 to selectively remove material from undoped silicon dioxide layer 22 to form undoped silicon dioxide caps 16 as seen in Figure 2.

A doped silicon dioxide layer 30 is deposited over multilayer structure 10 as a passivation layer. Preferably, doped silicon dioxide layer 30 is substantially composed of borophosphosilicate glass (BPSG), borosilicate glass (BSG), or phosphosilicate glass (PSG). Most preferably, doped silicon dioxide layer 30 is substantially composed of silicon dioxide having doping of about 3% or more for boron and about 3% or more for phosphorus. A photoresist layer 32 is applied over doped silicon dioxide layer 30. Photoresist layer 32 is processed to expose a second selected portion 17 of doped silicon dioxide layer 30 that is intended to be etched. Second selected portion 17 is seen in phantom in Figure 2.

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The structure seen in Figure 2 is now etched with a fluorinated or fluoro-carbon chemical etchant system to form second selected pattern 17 as illustrated in Figure 2. The preferred manner is an anisotropic plasma etch of doped silicon dioxide layer 30 down to the corresponding etch stop layer of undoped silicon dioxide cap 16. The plasma etch technique employed herein is preferably generated under a vacuum within the confines of a discharging unit and involves any type of a plasma system, including a high density plasma etcher. A conventional radio frequency reactive ion etcher (RF RIE) plasma system, a magnetically enhanced RIE (MERIE) plasma system, or an inductively coupled plasma system could be used. The preferred embodiment, however, is an RF type RIE or MERIE plasma system. It is preferred the plasma system being used has a plasma density in a range from about 10^9 /cm^3 to about 10^{11} /cm^3 A high density plasma system can also be used having a plasma density in a range from about 10^{12} /cm^3 to about 10^{13} /cm^3

One particular embodiment of a specific structure created utilizing the inventive process is illustrated in Figure 3 wherein a multilayer structure 50 is created that comprises a base silicon layer 12. Overlying silicon base layer 12 is a gate oxide layer 14 that covers silicon base layer 12. Gate oxide layer 14 may be relatively thin in comparison with the other layers of the multilayered structure. The next layer in multilayer structure 50 comprises a polysilicon gate layer 18. Overlying polysilicon gate layer 18 is a refractory metal silicide layer 20. A known benefit of refractory metal silicides is their low resistivity. Refractory metal silicide layer 20 may comprise any refractory metal including but not limited to titanium, tungsten, tantalum, and molybdenum. Preferably, refractory metal silicide layer 20 is substantially composed of tungsten silicide (WSi_x).

Overlying refractory metal silicide layer 20 is a substantially undoped silicon dioxide layer 22 which can be formed thermally, by plasma enhanced deposition, by a conventional TEOS precursor deposition that is preferably rich in carbon or hydrogen, or by a precursor of gaseous silane (SiH_4) with oxygen. The next layer in multilayer structure 50 is a

photoresist layer 24 that is processed to expose a first selected pattern 15 shown in phantom. Multilayer structure 50 is then etched according to first selected pattern 15 to selectively remove material so as to form gate stacks 26 as illustrated in Figure 4. Each gate stack 26 has an undoped silicon dioxide cap 52 thereon which was formed from undoped silicon dioxide layer 22.

A spacer 28 in on the sidewall of each gate stack 26. Spacers 28 are formed by subjecting a layer of silicon nitride deposited over gate stacks 26 to a spacer etch. Silicon nitride spacers 28 are generally perpendicular to silicon base layer 12. Alternatively, spacers 28 can be substantially composed of undoped silicon dioxide. As such, both spacers 28 and undoped silicon dioxide caps 52 can be made from the same materials and both act as an etch stop.

Once gate stacks 26 are formed, a contact 34 is defined therebetween upon silicon base layer 12. At this point in the processing, a doped silicon dioxide layer 30, composed of a material such as PSG, BSG, or BPSG, is deposited over multilayer structure 50. A photoresist layer 32 is then applied over doped silicon dioxide layer 30. Photoresist layer 32 is processed to create a second selected pattern 17 that is illustrated in phantom in Figure 4.

The structure seen in Figure 4 is now etched with a fluorinated or fluoro-carbon chemical etchant system according to second selected pattern 17. The preferred manner of etching of doped silicon dioxide layer 30 down to its corresponding etch stop layer, which is substantially undoped silicon dioxide layer 52, is by a plasma etch. The etch technique employed herein is preferably a plasma etch involving any type of a plasma system including a high density plasma etcher as previously discussed relative to Figure 2.

One factor that effects the etch rate and the etch selectivity of the process is pressure. The total pressure has a preferred range from about 1 millitorr to about 400 millitorr. A more preferred pressure range for a plasma etch is in a pressure range from about 1 millitorr to about 100 millitorr. The most preferred pressure range for a plasma etch is from about

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1 millitorr to about 75 millitorr. The pressure may be increased, however, above the most preferred ranges. For example, the RIE etch may be performed at about 100 millitorr. Selectivity can be optimized at a pressure range between about 10 millitorr and about 75 millitorr. Pressure increases may result in a loss in selectivity. The range in selectivity, however, can be adjusted to accommodate different pressures. As such, selectivity and pressure are inversely related.

Temperature is another factor that effects the selectivity of the etching process used. A preferable temperature range during the plasma etch has a range of about 10°C to about 80°C, and more preferably about 20°C to about 40°C. This is the temperature of a bottom electrode adjacent to silicon layer 12 during the etching process. The preferable range of the semiconductor materials is between about 40°C and about 130°C, and more preferably between about 40°C and about 90°C.

Undoped silicon dioxide cap 52 and silicon nitride spacers 28 protect gate stacks 26 from the fluorinated chemical etch. As illustrated in Figure 4, the etch will selectively and anisotropically remove doped silicon dioxide layer 30 above contact 34 as indicated by second selected pattern 17. The etch removes material from doped silicon dioxide layer 30 at a higher material removal rate than that of undoped silicon dioxide cap 52 and silicon nitride spacers or undoped silicon dioxide spacers 28. Preferably, the etch has a material removal rate for doped silicon dioxide is at least 10 times higher than that of undoped silicon dioxide. As such contact 34 is self-aligned between spacers 28 of gate stacks 26. The self-aligning aspect of contact 34 is due to the selectivity of the etch which assures that even in cases of misalignment of the exposure of second selected pattern 17, the fluorinated chemical etch through doped silicon dioxide layer 30 will properly place contact 34 on silicon base layer 12 and between adjacent silicon nitride spacers 28 that have been formed upon sides of gate stacks 26.

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Contact 34 is preferably exposed by an anisotropic plasma etch with a fluorinated chemistry that etches through BSG, PSG, BPSG, or doped silicon dioxide in general. The etch is preferably selective to undoped silicon dioxide, silicon, and silicon nitride. The fluorinated chemical etch utilizes a type of carbon fluorine gas from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_2F_8, CH_2F_2, CHF_3, C_2HF_5, CH_3F and combinations thereof. There are other fluorinated enchants in a substantially gas phase during the etching of the structure. An inert gas is often used in combination with the fluorinated etchant. Argon, nitrogen, and helium are examples of such an inert gas. The preferred gasses, however, are CF_4, CH_2F_2, CHF_3 and Ar. Alternatively CH_3F may be used in place of CH_2F_2. In particular, the preferred enchant is a fluorine deficient gas which is defined as a gas where there are not enough fluorine atoms to saturate the bonding for the carbon atoms.

A conductive material is formed upon contact 34 between spacers 28 within second selected pattern 17 as shown in Figure 4. The conductive material will form a contact plug to contact 34. It may be desirable to clad the contact plug with a refractory metal or a refractory metal silicide. As such, second selected pattern 17 would have proximate thereto the refractory metal or silicide thereof prior to formation of the contact plug in contact with contact 34.

The present invention has application to a wide variety of structures. The top layer of the gate stack, composed of undoped silicon dioxide, can be used to create and protect various types of structures during the doped silicon dioxide etching process for structures other than gate stacks.

The present invention allows the gate stack height to be reduced. One advantage of reducing the gate stack height is to reduce the process time which results in greater throughput. The reduced gate height results in a lower etch time and a reduced contact hole aspect ratio, the latter being defined as the ratio of height to width of the contact hole. By reducing the aspect ratio, or by reducing the height of the gate stack, there will be a decrease

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in the etch time. Another advantage of a lower gate stack height is that it reduces the overall topography which in turn results in it being easier to planarize and to use photolithographic processes. As such, the present invention increases yield.

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed and desired to be secured is:

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